

a refresh circuit controlling refreshing of said storage circuit; and
a memory control circuit comprising an address generation circuit
generating an address in said storage circuit to and from which the image data is written
in and read out,

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said memory control circuit comprising an area adjustment circuit which
sets up an additional area adjacent to an area in which the image data are actually
stored in a memory space of said storage circuit and storing therein data other than the
image data, which adjusts the address generated by said address generation circuit,
and which reads out the image data from said storage circuit, including the data in the
additional area, in response to the address and a read control signal supplied to said
storage circuit.

16. (New) An image processor comprising:

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a storage circuit storing therein image data;
a data input/output circuit controlling input/output of the image data;
an access control circuit controlling access of writing in and reading out
the image data to and from said storage circuit;
a refresh circuit controlling refreshing of said storage circuit; and
a memory control circuit comprising an address generation circuit
generating an address in said storage circuit to and from which the image data is written
in and read out, and generating an additional address of a width same as the address in

said storage circuit to and from which data other than the image data is written in and read out,

A2 said memory control circuit comprising an area adjustment circuit which sets up an additional area corresponding to the additional address and which is adjacent to an area in which the image data are actually stored in a memory space of said storage circuit and storing therein data other than the image data, which adjusts the address generated by said address generation circuit, and which reads out the image data from said storage circuit, including the data in the additional area, in response to the address and a read control signal supplied to said storage circuit.

17. (New) An image processing method comprising the steps of:

setting up, in a storage circuit in which image data is stored, an address space for a range of an image area in which the image data is written, and an additional address space of a width same as the address space for a range of an additional area which is adjacent to the image area and in which data other than the image data is written, with information supplied to a memory space of said storage circuit as a parameter;

writing the data other than the image data from external into the additional area in said storage circuit according to a first write control signal;

writing the image data at an address location of the image area in said storage circuit according to a second write control signal; and

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and reading out the data stored in the additional area and the image data
stored in the image area in said storage circuit in response to a first read control signal.
